## WE CLAIM:

1	1. A chemical vapor deposition (CVD) method for forming a compound comprising Ta
2	and N, comprising the steps of:
3	using an alkylimidotris(dialkylamido)Ta species for Ta precursor; and
4	providing a precursor supplying nitrogen.
1	2. The method of claim 1, further comprising the step of selecting
2	tertiaryamylimidotris(dimethylamido)Ta as said alkylimidotris(dialkylamido)Ta species.
1	3. The method of claim 1, further comprising the step of selecting ammonia for said
2	precursor supplying nitrogen.
1	4. The method of claim 1, further comprising the step of selecting said compound from
2	the group consisting of TaN and TaSiN.
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1	5. The method of claim 4, further comprising the step of selecting the N to Ta elemental
2	ratio in said compound to be greater than about 0.9.
1	6. The method of claim 4, further comprising the step of selecting a Si precursor for said
2	TaSiN from the group consisting of silane and disilane.

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7. The method of claim 1, further comprising the step of using hydrogen for carrier gas. 8. A semiconductor field effect device having a gate dielectric and a gate, wherein said 1 2 gate comprises a compound comprising Ta and N disposed over said gate dielectric, 3 wherein said compound has a resistivity below about  $20m\Omega cm$ , and wherein in said 4 compound the elemental ratio of N to Ta is greater than about 0.9. 9. The field effect device of claim 8, wherein said compound is TaN or TaSiN. 1 10. The field effect device of claim 9, wherein in said TaN the N to Ta elemental ratio is 1 2 between about 0.9 and 1.1. 1 11. The field effect device of claim 10, wherein said TaN has a crystalline material 2 structure. 1 12. The field effect device of claim 9, wherein in said TaSiN the Si to Ta elemental ratio 2 is between about 0.35 and 0.5. 1 13. The field effect device of claim 12, wherein said TaSiN has an substantially 2 amorphous material structure.

1	14. The field effect device of claim 9, wherein said TaSiN has a workfunction which
2	equals an n-doped Si workfunction within about 300mV.
1	15. The field effect device of claim 8, wherein said gate dielectric has an equivalent oxide
2	thickness of less than about 5nm.
1	16. The field effect device of claim 15, wherein said gate dielectric has an equivalent
2	oxide thickness of less than about 2nm.
1	17. The field effect device of claim 8, wherein said gate dielectric comprises SiO <sub>2</sub> .
1	18. The field effect device of claim 8, wherein said gate dielectric comprises a high-k
2	dielectric material.
1	19. The field effect device of claim 8, wherein said device is a Si based MOS transistor.
1	20. The field effect device of claim 19, wherein said device is an NMOS transistor.
1	21. The field effect device of claim 20, wherein said NMOS transistor has a threshold
2	voltage between about 0.15V and 0.55V.

1	22. A method for fabricating a semiconductor field effect device which has a gate
2	dielectric, comprising the step of depositing onto said gate dielectric a compound
3	comprising Ta and N by using chemical vapor deposition (CVD) with an
4	alkylimidotris(dialkylamido)Ta species for Ta precursor.
1	23. The method of claim 22, further comprising the step of selecting said compound with
2	a resistivity below about $20 m\Omega cm$ .
1	24. The method of claim 22, further comprising the step of selecting in said compound
2	the elemental ratio of N to Ta to be greater than about 0.9.
1	25. The method of claim 22, further comprising the step of selecting said compound from
2	the group consisting of TaN and TaSiN.
1	26. The method of claim 25, further comprising the step of selecting the N to Ta
2	elemental ratio in said TaN to be between about 0.9 and 1.1.
1	27. The method of claim 25, further comprising the step of selecting the Si to Ta
2	elemental ratio in said TaSiN to be between about 0.35 and 0.5

1	28. The method of claim 22, further comprising the step of selecting
2	tertiaryamylimidotris(dimethylamido)Ta as said alkylimidotris(dialkylamido)Ta species.
1	29. The method of claim 22, further comprising the step of heating said compound up to
2	about 1000°C.
1	30. The method of claim 22, further comprising the step of providing a source and a
2	drain, wherein the step of depositing said compound is carried out before the step of
3	providing said source and said drain.
1	31. The method of claim 22, further comprising the step of providing a source and a
2	drain, wherein the step of depositing said compound is carried out after the step of
3	providing said source and said drain.
1	32. The method of claim 22, wherein said step of depositing is carried out conformally
2	onto a patterned surface.
1	33. A processor, comprising:
2	at least one chip, wherein said chip comprises at least one semiconductor field
3	effect device having a gate dielectric and a gate, wherein said gate comprises a compound
1	comprising Ta and N disposed over said gate dielectric, wherein said compound has a

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- resistivity below about  $20m\Omega cm$ , and wherein in said compound the elemental ratio of N to Ta is greater than about 0.9.
- 1 34. The processor of claim 33, wherein said processor is a digital processor.
- 1 35. The processor of claim 33, wherein said processor comprises at least one analog circuit.